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10/604,912	08/26/2003	Heemyoung Park	FIS920030026US1	1911

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EXAMINER	
KEBEDE, BROOK	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 01/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/604,912	PARK ET AL.	
	Examiner	Art Unit	
	Brook Kebede	2823	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 January 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,2,4-9,11-17,19-24 and 26-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2,4-9,11-17,19-24 and 26-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on January 3, 2006 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1, 2, 4-9, 11-17, 19-24 and 26-28 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (US/6,429,084).

Re claim 1, park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate (i.e., SOI substrate), a gate conductor (50) above the substrate (see Fig. 1), and at least one sacrificial layer (51 52 54) above the gate conductor (50); patterning the laminated structure into at least one gate stack (55) extending from the substrate (see Fig. 1) (Col. 1, lines 50-65); forming spacers (60 70) to have a target spacer width adjacent said gate stack (55) (see Fig. 2), wherein by forming the gate stack form the laminated structure with the at least one sacrificial layer, as opposed to without the at least one sacrificial layer, a height of the gate stack is increased so that the target spacer can be achieved; doping regions of the substrate not protected

by the spacers (60 70) with an impurity to form source and drain regions adjacent the gate stack (55); wherein the spacers with the target spacer width separate the source drain regions form that gate stack so to avoid lateral encroachment of the impurity into a channel region below the gate stack; and removing the spacers and the sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 2, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein forming of the spacers adjacent the gate stack comprises forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 4, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming of comprises the spacers so as to positions the source and drain regions further from the gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 5, The method in claim 1, wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 6, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 7, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below

said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 8, as applied to claim 1 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 9, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, the method comprising: forming a laminated structure having a substrate (see Fig. 1), a gate conductor (50) above the substrate, and at least one sacrificial layer (54) above said gate conductor (see Fig. 1); patterning said laminated structure into at least one

gat stack extending from said substrate; forming spacers to have a target spacer width adjacent gate stack wherein by forming the gate stack form the laminated structure with the at least one sacrificial layer, as opposed to without the at least one sacrificial layer, a height of the gate stack is increased so that the target spacer can be achieved; epitaxially growing raised source and drain regions on said substrate adjacent said gate stack (see Fig. 5); after said epitaxially growing of said raised source drain regions, implanting an impurity into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurity after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 11, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming the spacers comprises forming of the spacers with target spacer width so as to positions said raised source and drain regions further from said gate conductor when compared to raised source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 12, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming

additional sacrificial layers above said oxide layer, wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 13, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 14, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a dielectric layer (40) below said gate conductor layer (50) a silicon layer below said gate dielectric layer (40), wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity to that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and aid gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 15, as applied to claim 9 above, Park et al. disclose all the claimed limitations including the limitation wherein by implanting said impurity after said epitaxially growing process, said impurity avoid being diffused as result of said thermal budget of said epitaxially growing process (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 16, Park et al. disclose a method of forming an integrated circuit transistor having a reduced gate height, said method comprising: forming a laminated structure having a substrate, a gate conductor above said substrate, and at least one sacrificial layer above said gate conductor; patterning said laminated structure into at least one gate stack extending from said substrate; forming spacers to have a target spacer width adjacent said gate stack, wherein by forming the gate stack form the laminated structure with the at least one sacrificial layer, as opposed to without the at least one sacrificial layer, a height of the gate stack is increased so that the target spacer can be achieved; epitaxially growing raised source and drain regions on said substrate adjacent said spacers, wherein said process of epitaxially growing said raised source and drain regions is performed in the absence of doping impurities; after said epitaxially growing of said raised source drain regions, implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity unto a channel region below the gate stack; and removing said spacers and said sacrificial layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 17, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein forming of the spacers adjacent the gate stack comprises forming of the spacers adjacent the gate conductor and at least on sacrificial oxide layer (54) above the gate conductor (50) (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 19, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein the forming the spacers comprise forming the spacers with target spacer so as to positions said source and drain regions further from said gate conductor when compared to source and drain regions formed with spacers formed only to said height of said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 20, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial layer above said gate conductor is formed in a process comprising: forming a sacrificial oxide layer above said gate conductor, and forming additional sacrificial layers above said oxide layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 21, as applied to claim 20 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 22, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer (i.e., part of SOI) below said gate conductor (50), wherein said method further comprises doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein the combined height of said gate conductor and said sacrificial layer prevents said impurity from

reaching said silicon layer, and whereas, without said sacrificial layer, said doping process would implant an impurity through said gate conductor and said gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 23, as applied to claim 16 above, Park et al. disclose all the claimed limitations including the limitation wherein said laminated structure includes a gate dielectric (40) below said gate conductor layer and a silicon layer below said gate dielectric layer , wherein said method further comprises a first doping process of doping said source and drain regions and said gate conductor together in a self-aligned implantation after said patterning process, wherein said method further comprises a second doping process of doping halo regions below said gate conductor in a self-aligned implantation with an impurity of an opposite polarity that used in said first doping process after said first doping process, wherein the combined height of said gate conductor and said sacrificial layer prevents impurities from reaching said silicon layer, and whereas, without said sacrificial layer, said doping processes would implant impurities through said gate conductor and gate dielectric layer to said silicon layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 24, Park et al. disclose a method of producing an integrated circuit transistor comprising: forming a laminated stack deposition, wherein said laminated stack deposition is formed in a process comprising: forming a silicon layer over a substrate layer (30) (i.e., part of SOI); forming a gate oxide (40) on said silicon layer (30); forming a gate conductor (50) on said gate oxide (40); and forming of least one sacrificial material above said gate conductor, patterning said gate oxide (see Figs. 5 and 6), gate conductor, and said sacrificial material into at least one gate stack (see Figs. 1-6); forming temporary spacers (70 60) to have a target width adjacent said gate stack (55), wherein by forming the gate stack form the laminated structure

with the at least one sacrificial layer, as opposed to without the at least one sacrificial layer, a height of the gate stack is increased so that the target spacer can be achieved; epitaxially growing raised source and drain regions (36) (see Fig. 6) above said substrate layer adjacent said temporary spacers, such that said temporary spacers separate said raised source and drain regions from said gate stack, wherein the epitaxially growing process of the raised source and drain regions performed in the absence of doping of impurities; simultaneously implanting impurities into said raised source and drain regions and into said substrate below the raised source drain regions (see Figs. 9 and 10); wherein implanting said impurities after said epitaxially growing and raised source drain regions avoids subjecting said impurities to the thermal budget of said epitaxially growing process and wherein said target spacer width separate the raised source drain regions form the gate stack so as to avoid lateral encroachment of the impurity into a channel region below the gate stack; growing an additional dielectric layer (44) (see Fig. 8) on said raised source and drain regions (36); removing said temporary spacers (see Fig. 9) without removing said sacrificial material (51) ; performing a halo implant (see Fig. 10) in said raised source and drain regions and in exposed regions of said silicon layer; forming a permanent spacer (80) (see Fig. 11) adjacent said gate stack, wherein said permanent spacer is thinner than said temporary spacer; performing a source and drain extensions implant in said raised source and drain regions and exposed regions of said silicon; forming a final spacer filling said exposed regions of said silicon between said permanent spacer and said raised source and drain regions; implanting additional impurity into said raised source and drain regions and exposed regions of said silicon; annealing to activate all impurity; etching back said additional dielectric layer on said raised source and drain regions; and saliciding both said gate conductor and said raised source and drain regions (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 26, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said removing of said sacrificial layer reduces the height of said gate conductor relative to the gate height associated with the spacing of the source and drain regions created by said spacers (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 27, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said forming of said sacrificial material above said gate conductor further comprises forming a sacrificial oxide layer above said gate conductor, forming a sacrificial nitride layer above said oxide layer and forming a sacrificial hard insulator material above said nitride layer (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Re claim 28, as applied to claim 24 above, Park et al. disclose all the claimed limitations including the limitation wherein said sacrificial oxide layer protects said gate conductor (see Figs. 1-12 and related text Col. 1, line 50 – Col. 3, line 20).

Response to Arguments

4. Applicants' arguments filed on January 3, 2006 have been fully considered but they are not persuasive.

With respect to claims rejection under 35 U.S.C. § 102, applicants ague that "Park discloses the formation of temporary spacers adjacent the gate stack; however, the width of the temporary spacers is set to define the area for the halo and extensions implants… Park does not address the issue of the lateral encroachment…"

In response applicants' argument, it is respectfully submitted that Park et al. '084 disclose all the claimed limitations as applied in Paragraph 3above. In addition, Park et al. disclose all the limitations including forming of the target spacer. As shown Figs. 1-4, the target spacers (42 60 70) are formed to protect the gate electrode and the channel region under the gate electrode

during amorphization ion implant process (see Figs. 2 and 3) prior implanting the S/D implant. In addition, none the drawing show diffusion of the impurities under the gate conductor (i.e., in the channel region) as shown in Figs. 5-8. As shown Fig. 5, the target spacer protects the channel region for impurities during the S/D implantation process. Furthermore, it is respectfully submitted that the lateral encroachment never occur in Park et al. '084 disclosure because the use of spacer as well dummy spacer is intended to avoid such problem. This is the art recognized problem so that Park et al. '084 process also intended to avoid such problem.

Applicants further argue that "Park does not teach or suggest after epitaxially growing raised source and drain regions, implanting impurities into the raised source and drain regions and into said substrate below the raised source and drain regions, wherein implanting the impurities after epitaxially growing the raised source and drain regions avoids subjecting the impurities to the thermal budget of the epitaxially grown..."

In response to applicants' argument, it is respectfully submitted that the implant form S/D extension is conducted after the epitaxial layer formed (see Figs. 9 and 10). Furthermore, the impurities **35'** below the epi-layer **36** (see Fig. 10) is occurred due to the implantation process after the epitaxial layer **36** is formed and does not required any heating (annealing) process to diffuse the dopant into the epitaxial layer **36** as shown in Fig. 10 (i.e., wherein implanting the impurities after epitaxially growing the raised source and drain regions avoids subjecting the impurities to the thermal budget of the epitaxially grown).

Furthermore, claims are to given their broadest reasonable interpretation in light of the supporting disclosure. See *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997). Limitations appearing in the specification but not recited in the claim are not

read into the claim. See *In re Prater*, 415 F.2d 1393, 1404-05, 162 USPQ 541, 550-551 (CCPA 1969). See also *In re Zletz*, 893 F.2d 319, 321-22, 13 USPQ2d 1320, 1322 (Fed. Cir. 1989).

Therefore, the rejection of claims 1-28 under 35 U.S.C. § 102 is sill deemed proper.

Conclusion

5. Applicants' amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Correspondence

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Brook Kebede whose telephone number is (571) 272-1862. The examiner can normally be reached on 8-5 Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Brook Kebede

Brook Kebede
Primary Examiner
Art Unit 2823

BK
January 23, 2006